# DECLARATION

I, Young Woo Park, Korean Patent Attorney of 5F, Seil Building, 727-13, Yoksam-dong, Gangnam-gu, Seoul, Korea do hereby solemnly and sincerely declare as follows:

1. That I am well acquainted with the English and Korean languages.

2. That the following is a correct translation into English of the accompanying certified copy of a Korean Patent Application No. 2002-56070.

and I make the solemn declaration conscientiously believing the same to be true.

Seoul, May 22, 2006

Young Woo Park

Young-Woo PARK

THE KOREAN INDUSTRIAL

PROPERTY OFFICE

This is to certify that annexed hereto is a true copy from the records of the Korean Industrial Property Office of the following application as filed.

Application Number: Patent Application No. 2002-56070

Date of Application: September 16, 2002

Applicant : Samsung Electronics Co., Ltd.

**COMMISSIONER**

**PATENT APPLICATION**

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Title of the Invention : LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURING THE SAME

Dated this: August 22, 2003

To the COMMISSIONER

[ABSTRACT]

[ABSTRACT]

A substrate for a display device has a reduced size and weight. Connecting lines are formed on peripheral region adjacent to display region of a display device, and scan driving signal is applied to scan lines through the connecting lines. The connecting lines includes first connecting lines and second connecting lines. The first connecting lines are formed in a same layer as the scan lines, and the second connecting lines are formed in a same layer as the data lines. The total area of the wirings formed in the peripheral region is reduced, and the size and weight of the liquid crystal display device may be reduced.

[REPRESENTATIVE FIGURE]

FIG. 1

[SPECIFICATION]

[TITLE OF THE INVENTION]

LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURING THE SAME

[BRIEF EXPLANATION OF THE DRAWINGS]

FIG. 1 is a sectional view showing an LCD device according to one exemplary embodiment of the present invention;

FIG. 2 is a plan view showing a thin film transistor (TFT) substrate according to one exemplary embodiment of the present invention;

FIG. 3 is a partially enlarged view of FIG. 2;

FIG. 4 is a sectional view taken along the line A-A' of FIG. 3;

FIG. 5 is a sectional view taken along the line B-B' of FIG. 3;

FIGS. 6A-6E are sectional views showing one exemplary method of manufacturing the TFT substrate of FIG. 5;

FIG. 7 is a plan view showing a TFT substrate according to another exemplary embodiment of the present invention; and

FIG. 8 is a partially enlarged view of FIG. 7.

<EXPLANATION ON CHIEF REFERENCE NUMERALS OF DRAWINGS >

100 : TFT substrate

110 : first substrate

120 : second substrate

130 : pixel electrode

150 : driving circuit

200 : C/F substrate

300 : liquid crystal layer

400 : liquid crystal display apparatus

GL : gate line

DL : data line

GW : connecting line

[DETAILED DESCRIPTION OF THE INVENTION]

[PURPOSE OF THE INVENTION]

[THE ART TO WHICH THE INVENTION PERTAINS AND THE PRIOR ART]

The disclosure relates to a substrate used for a display device, a liquid crystal display device, and a method of manufacturing the liquid crystal display (LCD) device, more particularly to a substrate used for a display device, a liquid crystal display device, and a method of manufacturing the liquid crystal display device that has a reduced size and weight.

In these days such an information society, an electronic display device gets more important, and is used in various industrial field. An electronic device is defined that a

device converts an electronic information signal of various electronic devices into light information signal, that is visible by human sight.

As improving the semiconductor technique, the request for a flat display device is increasing. A liquid crystal display device among the flat display device is thin and light as compared with the other display devices, and needs low consumption power and low driving voltage, so that the liquid crystal display device is used in the various field.

In general, the liquid crystal display device includes a liquid crystal display panel for displaying an image, and the liquid crystal display panel has a first substrate, a second substrate and a liquid crystal layer interposed between the first and second substrate. A driver printed circuit board used for driving the liquid crystal display panel is electrically connected to the liquid crystal display panel through a tape carrier package (TCP).

The driver printed circuit board includes a data printed circuit board and a gate printed circuit board. The data printed circuit board drives a plurality of data lines formed on the liquid crystal display panel, and the gate printed circuit board drives a plurality of scan lines (or gate lines) formed on the liquid crystal display panel. The data printed circuit board is electrically connected with the data lines through a data side TCP, and the gate printed circuit board is electrically connected with the scan lines through a gate side TCP. A data driver chip is disposed in the data side TCP, and a scan driver chip (or a gate driver chip) is disposed in the gate side TCP.

Recently, a scan driver circuit (or gate driver circuit) is formed on the liquid crystal display panel so that the number of steps for manufacturing the liquid crystal display

device may be reduced. The scan driver circuit provides the scan lines with a scan driving signal.

Particularly, the first substrate or the second substrate of the liquid crystal display panel includes a display region and a peripheral region. A data driving circuit is formed in a first peripheral region having an end portion of the data line. A scan driving circuit is formed in a second peripheral region having an end portion of the scan line and adjacent to the first peripheral region. Therefore, a data signal from the data driving circuit is applied to the data line, a data signal from the scan driving circuit is applied to the scan line.

However, since the scan driver circuit is formed at first ends of the scan lines, the liquid crystal display panel does not have symmetric structure. When another space is provided at second ends of the scan lines so as to provide symmetric structure, the size of the liquid crystal display device may increase.

Moreover, to solve the above problem, the scan driving circuit and the data driving circuit are formed in the first peripheral area, thereby, only the scan connecting lines connecting the scan line with the scan driving circuit is formed in the second peripheral area. However, the number of the scan connecting lines is equal to the number of the scan lines, so that the width of the second peripheral area is limited. Therefore, to reducing the size of the liquid crystal display device is limited.

[TECHNICAL OBJECT OF THE INVENTION]

The first object of the present invention is to provide a liquid crystal display device that has a reduced size and weight.

The second object of the present invention is to provide a method for manufacturing the liquid crystal display device that has a reduced size and weight.

[CONTRUCTION AND OPERATION OF THE INVENTION]

According to one aspect of the present invention to accomplish the first feature of the invention, there is provided a liquid crystal display device, the liquid display device includes a first substrate including a display region and a peripheral region adjacent to the display region, the display region having a plurality of pixels, a plurality of data lines and a plurality of scan lines, a second substrate facing the first substrate and a liquid crystal layer disposed between the first and second substrate; a driver section including a scan driver circuit and a data driver circuit, the scan driver circuit and the data driver circuit formed in a first peripheral region of the peripheral region, the scan driver circuit providing the scan lines with a scan driving signal, and the data driver circuit providing the data lines with a data signal; a plurality of first connecting lines connected with a first end portion of the scan lines in a second peripheral area adjacent to the first peripheral area, and applying the scan driving signal, and divided into a plurality of groups, and wherein each of the groups are disposed the different layer from each other; and a plurality of data wirings connected with the data line in the first peripheral area, and applying the data driving signal.

To accomplish the second feature of the invention, there is provided a method of manufacturing a liquid crystal display device.

A plurality of scan lines, a plurality of scan electrode extended from the scan lines in display area of a first substrate, and a plurality of first scan connecting lines

electronically connected with a portion of the scan lines in a peripheral area of the display area are formed; An insulation layer on the first substrate having the scan line, the scan electrode and the first connection lines is formed; A plurality of data lines, a plurality of source and drain electrodes extended from the data lines, and a plurality of second connecting lines electronically connected with the remaining portion of the scan lines in a peripheral area of the display area are formed; The first substrate with a second substrate are combined; and A liquid crystal between the first and second substrates is interposed.

According to the liquid crystal display device and the method of manufacturing the same, the scan connecting line includes the first scan connecting line formed from substantially the same layer as the scan line in the display area and the second scan connecting line formed substantially the same layer as the data line. Therefore, the weight and size of the liquid crystal display device may be reduced.

Hereinafter the preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings.

FIG. 1 is a sectional view showing an LCD device according to one exemplary embodiment of the present invention.

Referring to FIG. 1, a liquid crystal display device 400 includes a liquid crystal display panel, and the liquid crystal display panel includes an TFT substrate 100, a color filter (C/F) substrate 200 facing the TFT substrate 100, and a liquid crystal layer 300 interposed between the TFT substrate 100 and the C/F substrate 200. The liquid crystal display panel has a display region (D) and first and second peripheral regions (S1,

S2). An image is displayed through the display region D, and the first and second peripheral regions (S1, S2) are disposed adjacent to the display region D.

Particularly, the TFT substrate 100 includes a plurality of scan lines (or gate lines, not shown) and a plurality of data lines (not shown). The scan lines and data lines are formed on a first substrate. Pixel regions (or pixels) are defined by the scan lines and the data lines. The pixel regions respectively include a TFT 120 and a pixel electrode 140 connected to the TFT 120.

In addition, the TFT substrate 100 includes a plurality of connecting lines GW. The connecting lines are formed in the second peripheral region S2, and an external scan driving signal is sequentially applied to the scan lines. The connecting lines GW include a first connecting line GW1 and a second connecting line GW2. The first connecting line GW1 is formed from the same layer as the gate electrode of the TFT 120, and the second connecting line GW2 is formed from the same layer as the source electrode and the drain electrode. Since the connecting lines GW have double layers, the width (W) of the second connecting line GW2 may be reduced.

The C/F substrate 200 includes a color filter 220,a shielding layer 230 and a common electrode 240. The color filter 210 is formed on the second substrate 210 and the color filter 220 faces the display region D. The shielding layer 230 is formed on the second substrate 210 to face the second peripheral region S2. The common electrode 240 is uniformly formed on the color filter 220 and the shielding layer 230.

After the TFT substrate 100 and the C/F substrate 200 are disposed such that the common electrode 240 and the pixel electrode 140 face each other, the TFT substrate

100 are fixed to the C/F substrate 200 by means of sealant 350. Liquid crystal is interposed between the TFT substrate 100 and the C/F substrate 200 to form the liquid crystal layer 300, so that the liquid crystal display device 400 is manufactured.

FIG. 2 is a plan view showing a thin film transistor (TFT) substrate according to one exemplary embodiment of the present invention, and FIG. 3 is a partially enlarged view of FIG. 2.

Referring to FIGS. 2 and 3, the TFT substrate 100 includes a display region (D) and first and second peripheral regions (S1, S2). The first and second peripheral regions (S1, S2) are formed adjacent to the display region D.

A plurality of scan lines (SL, or gate lines GL) and a plurality of data lines (DL) are formed on the display region D. The scan lines are extended in a first direction, and the data lines (DL) are extended in a second direction substantially perpendicular to the first direction. Pixel regions (or pixels) are defined by the scan lines and the data lines, and the pixel regions respectively include a TFT 120 and a pixel electrode 140 connected to drain electrode of the TFT 120. Ends of the scan lines are disposed on the second peripheral region S2, and ends of data lines DL are disposed on the first peripheral region S2.

The TFT 120 includes a gate electrode 121, a source electrode 125 and a drain electrode. The gate electrode 121 is insulated from the source electrode 125 and the drain electrode 126 by means of the gate insulation layer 122. An active pattern 123 and an ohmic contact pattern (or contact pattern) 124 are formed on the gate insulation layer 122. The data signal is applied to the drain electrode from the source electrode

through the active pattern 123 and ohmic contact pattern 124. Hereinafter, the active pattern 123 and ohmic contact pattern 124 is referred to as a semiconductor layer. The drain electrode 126 and the source electrode 125 are formed on the ohmic contact pattern 124. The source electrode 125 is spaced apart from the drain electrode 126.

An organic insulation layer 130 is formed on the TFT 120. A first contact hole 131 is formed on the organic insulation layer 130. The first contact hole 131 exposes the drain electrode 126 and electrically connects between the drain electrode 126 and pixel electrode 140 formed on the organic insulation layer 130.

A driving circuit 150 is formed in the second peripheral region S2. The driving circuit 150 includes a gate driving circuit and a data driving circuit. The gate driving circuit generates a gate driving signal provided to the gate line GL and driving the TFT 120. The data driving circuit generates a data driving signal provided to the data line DL and applied to the pixel electrode 140.

As shown in FIGS. 3 to 5, Connecting lines GW are formed in the second peripheral region S2. The connecting lines GW provide the scan lines with the scan driving signal outputted from the scan driver circuit. There is a one-to-one correspondence between the connecting lines GW and the scan lines (SL; or gate lines GL).

The connecting lines GW include a plurality of first connecting lines GW1 and a plurality of second connecting lines GW2. The first connecting lines GW1 are formed in a same layer as the gate electrode 121 and scan lines, and the second connecting lines GW2 are formed from the same layer as the data lines, source electrode 125 and the

drain electrode 126. The first connecting lines GW1 are electrically insulated from the second connecting lines GW2 by means of the gate insulation layer 122. The first connecting line is electrically connected to odd numbered scan lines, and the second connecting lines are electrically connected to even numbered scan lines.

In addition, each of the second connecting lines GW2 may be disposed between two first connecting lines and partly overlap with two first connecting lines. When the second connecting lines GW2 is disposed in the space between two first connecting lines GW1, the first horizontal distance between an edge of the first connecting line GW1 and an edge of the second connecting line GW2 is referred to as 'd1', the second horizontal distance between adjacent two first connecting lines is referred to as 'd2', d1 is less than (d2 – w) /2.

The vertical distance between the first connecting lines is spaced apart by a predetermined distance. The vertical distance between the second connecting lines is also spaced apart by a predetermined distance. The vertical distance between the first and second connecting lines is also spaced apart by a predetermined distance. Therefore, electrical short between connecting lines may be prevented, and capacitance between connecting lines may be reduced.

An insulating interlayer 127 is formed between the second gate wiring GW2 and the gate insulating layer 122 corresponding to the second gate wiring GW2. The insulating interlayer 127 is formed simultaneously when the active pattern 123 of the TFT 120 and an ohmic contact pattern 124 are formed. An organic insulating layer 130 is formed on the gate insulating layer 122 and the second gate wiring GW2

As shown in FIGS. 3 and 5, since the first connecting lines GW1 are formed from the same layer as the gate electrode 121 and the scan lines, each of the first connecting lines GW1 is connected to the corresponding scan line. Since the second connecting lines GW2 are formed from the same layer as the source electrode 125 and the drain electrode 126, each of the second connecting lines GW2 is electrically connected to the corresponding scan line through a second contact hole 127a. The second contact hole 127a is formed at the insulating interlayer 127 and the gate insulation layer 122 both of which are formed under the second connecting lines GW2. The second contact hole 127a exposes ends of the even numbered scan lines. The second connecting lines GW2 are electrically connected to ends of the even numbered scan lines exposed by the second contact hole 127a.

FIGS. 6A-6E are sectional views showing one exemplary method of manufacturing the TFT substrate of FIG. 5.

Referring to FIG. 6A, a first metallic layer (not shown) having aluminum (Al), chrome (Cr) or molybdenum tungsten (MoW) is spread by sputtering method on the first substrate 110 having insulation substance such as glass or ceramic. By patterning the first metallic layer, the gate ling GL extended in the first direction and the gate electrode 121 separated from the gate line GL are formed in the display area D by patterning the first metallic layer, and the first gate wiring GW1 connected to the odd-number gate line GL and separated from the each other is formed in the second peripheral area S2.

Referring to FIG. 6B, a silicon nitride layer is formed on the first substrate 110 on which the gate electrode 121, scan line and the first connecting lines GW1, thereby

forming a gate insulation layer 122. The silicon nitride layer is formed by a plasma chemical vapor deposition method.

Referring to FIG. 6C, the ohmic contact layer 113 and the active layer 112 are patterned to form a semiconductor layer 130, i.e. an active pattern 123 and an ohmic contact pattern 124, on the gate insulation layer 120 under which the gate electrode 105 is positioned. The active pattern 123 comprises amorphous silicon layer, and the ohmic contact pattern 124 comprises n+ doped amorphous silicon layer.

In addition, an insulating interlayer 127 comprising the active pattern 123 and the ohmic contact pattern 124 is formed on the gate insulation layer 112 to be disposed between the first connecting lines GW1.

The thickness of the regions between the first connecting lines GW1 is uniformized by the insulating interlayer 127. In addition, since the second connecting lines GW2 are spaced apart from the first connecting lines by the insulating interlayer 127, the parasitic capacitance between the first and second connecting lines GW1 and GW2 is reduced.

A second contact hole 127a is formed on the insulating interlayer 127 and the gate insulation layer 122 by a photolithography method using a second photomask (not shown). The second contact hole 127a exposes ends of the even numbered scan lines so that the second connection lines GW2 are electrically connected to the even numbered scan lines.

Referring to FIG. 6D, a second metal such as chrome (Cr) is deposited on the first substrate 110 on which the gate insulation layer 122 and the insulating interlayer 127 to from a second metal layer 114 by a sputtering method. The second metal layer 114 is

patterned to form a data line DL extended in a second direction in perpendicular to the first direction, a source electrode 125 and a drain electrode 126 separated by the data line DL on the display region D. At the same time, second connecting lines GW2 are formed on the second peripheral region S2. Each of the second connecting lines S2 is electrically connected to the corresponding even numbered scan lines through the second contact hole.

The ohmic contact pattern 124 is removed by a reactive ion etching (RIE) method. Then, the active pattern region is exposed between the source electrode 125 and drain electrode 127.

Therefore, the TFT 120, which includes the gate electrode 121, the active pattern 123, the ohmic contact pattern 124, the source electrode 125 and the drain electrode 126, are formed in the display region D. In addition, the first and second connecting lines GW1 and GW2 are formed in the second peripheral region S2.

Each of the second connecting lines CL2 may be disposed between two adjacent first connecting lines and may partly overlap with two first connecting lines. When the second connecting line GW2 is disposed between the two first connecting lines GW1, the first horizontal distance between an edge of the first connecting line GW1 and an edge of the second connecting line GW2 is referred to as 'd1', the second horizontal distance between adjacent two first connecting lines is referred to as 'd2', d1 is less than (d2 – w) /2. Therefore, a width of the connecting lines GW on the first substrate 110 is reduced, and a size of the second peripheral area S2 is reduced

Referring to FIG. 6E, a photosensitive organic resist such as an acryl resin is coated on the whole surfaces of the display region D and the second peripheral region S2 of the first substrate 110 by a spin coating method or a slit coating method, so that an photosensitive organic insulation layer is formed. Then, the photosensitive organic insulation layer is exposed and is developed by means of a fourth mask (not shown) to form an organic insulation layer 130 having a first contact hole 131. The first contact hole 131 exposes the drain electrode 126 of the TFT 120.

Referring again to FIG. 5, a transparent conductive film such as indium tin oxide (ITO) or indium zinc oxide (IZO) is deposited on the drain electrode 126 that is exposed by the organic insulation layer 130 and the first contact hole 131. The transparent conductive film is patterned via a photolithography process using a fifth photomask (not shown) to form a pixel electrode 140 on the display region D. The pixel electrode 140 is electrically connected to the drain electrode 126 through the first contact hole 131.

FIG. 7 is a plan view showing a TFT substrate according to another exemplary embodiment of the present invention, and FIG. 8 is a partially enlarged view of FIG. 7.

Referring to FIGS. 7 and 8, the TFT substrate 100 includes a first peripheral region S1, a second peripheral region S2 and a third peripheral region S3. The first, second and third peripheral regions (S1, S2, S3) are formed adjacent to the display region D. A plurality of scan lines (SL, or gate lines GL) and a plurality of data lines (DL) are formed on the display region D. The scan lines are extended in a first direction, and the data lines (DL) are extended in a second direction substantially perpendicular to the first direction.

First ends of the scan lines are disposed on the second peripheral region S2, first ends of data lines DL are disposed on the first peripheral region S1, and second ends of the scan lines are disposed on the third peripheral region S3.

A driver section 150 is arranged in the first peripheral region S1. The driver section 150 may be a driver chip. The driver section 150 includes a first scan driver circuit (or a first gate driver circuit), a second scan driver circuit (or a second gate driver circuit) and a data driver circuit. The first scan driver circuit sequentially provides the odd numbered scan lines (or gate lines) with a first scan driving signal. The second scan driver circuit sequentially provides the even numbered scan lines (or gate lines) with a second scan driving signal. The data driver circuit provides the data lines with a data signal.

In addition, left connecting lines LGW are formed in the second peripheral region S2. The left connecting lines LGW provides the odd numbered scan lines with the first scan driving signal outputted from the first scan driver circuit. The left connecting lines LGW includes first connecting lines LGW1 and second connecting lines LGW2. The first connecting lines LGW1 are formed from the same layer as the gate electrode 121, the second connecting lines LGW2 are formed from the same layer as the drain electrode 126. The first connecting lines LGW1 and the second connecting lines LGW2 are insulated from each other by means of the gate insulation layer 122. The first connecting lines LGW1 and the second connecting lines LGW2 are alternately connected to odd numbered scan lines.

Right connecting lines RGW are formed in the third peripheral region S3. The right connecting lines RGW provides the even numbered scan lines with the second

scan driving signal outputted from the second scan driver circuit. The right connecting lines RGW includes third connecting lines RGW1 and fourth connecting lines RGW2. The third connecting lines RGW1 are formed from the same layer as the first connecting lines LGW1, the fourth connecting lines RGW2 are formed from the same layer as the second connecting lines LGW2. The third connecting lines RGW1 and the fourth connecting lines RGW2 are alternately connected to even numbered scan lines.

Each of the second connecting lines LGW2 may be disposed between two first connecting lines and partly overlap with two first connecting lines LGW1. When the second connecting line LGW2 is disposed between the two first connecting lines LGW1, the first horizontal distance between an edge of the first connecting line LGW1 and an edge of the second connecting line LGW2 is referred to as 'd1', the second horizontal distance between adjacent two first connecting lines is referred to as 'd2', d1 is less than (d2 – w) /2. In addition, each of the fourth connecting lines RGW2 may be disposed between two third connecting lines and partly overlap with two third connecting lines RGW1.

Therefore, the width of the second peripheral region S2 and the width of the third peripheral region S3 are reduced, and the total area of the peripheral region of the liquid crystal display device may be reduced.

In FIGS. 7 and 8, each of the first and second gate driving circuit drives each of two divided gate lines GL in accordance with one embodiment of the present invention. However, in accordance with another embodiment, a gate line ma be divided into two, the left connecting line LGW may apply the first gate driving signal as a left end portion,

and the right connecting line RGW may apply the second gate driving signal as a right end portion.

[EFFECT OF THE INVENTION]

According to the present invention, a connecting line includes a first connecting line formed in the same layer as a gate line formed in a display area and a second connecting line formed in the same layer as a a data line.

Thereby, a size of a peripheral area having the connecting line is reduced, and a size and a weight of the liquid crystal display apparatus may be reduced.

Moreover, even though the first and second connecting lines are formed in the different layer from the each other, the first and second connecting line are formed simultaneously when the gate line and data line are formed. Thereby, the connecting lines are formed without any further process, and an additional process may be preventable.

This invention has been described with reference to the exemplary embodiments. It is evident, however, that many alternative modifications and variations will be apparent to those having skill in the art in light of the foregoing description. Accordingly, the present invention embraces all such alternative modifications and variations as fall within the spirit and scope of the appended claims.

[CLAIMS]

[CLAIMS 1]

A liquid crystal display device comprising:

a liquid crystal panel including;

a first substrate including a display region and a peripheral region adjacent to the display region, the display region having a plurality of pixels, a plurality of data lines and a plurality of scan lines;

a second substrate facing the first substrate; and

a liquid crystal layer disposed between the first and second substrate;

a driver section including a scan driver circuit and a data driver circuit, the scan driver circuit and the data driver circuit formed in a first peripheral region of the peripheral region, the scan driver circuit providing the scan lines with a scan driving signal, and the data driver circuit providing the data lines with a data signal;

a plurality of first connecting lines connected with a first end portion of the scan lines in a second peripheral area adjacent to the first peripheral area, and applying the scan driving signal, and divided into a plurality of groups, and wherein each of the groups are disposed the different layer from each other; and

a plurality of data wirings connected with the data line in the first peripheral area, and applying the data driving signal.

[CLAIMS 2]

The display device of claim 1, wherein the first connecting part includes:

a first group having a plurality of first connecting lines formed from a same layer as the scan lines; and

a second group having a plurality of second connecting lines formed from a same layer as the data lines.

[CLAIMS 3]

The display device of claim 2, wherein each of the first connecting lines partly overlaps with at least one of the second connecting lines.

[CLAIMS 4]

The display device of claim 2, wherein the substrate further comprises a first insulation layer, interposed between the first and second connecting lines, for electrically insulating the first connecting lines from the second connecting lines.

[CLAIMS 5]

The display device of claim 4, wherein the switching device comprises a thin film transistor, and the insulation layer comprises a scan insulation layer insulating the gate electrode, the source electrode and the drain electrode of the switching device, the semiconductor layer of the switching device.

[CLAIMS 6]

The display device of claim 4, wherein the first insulation layer includes a contact hole for exposing the first ends of at least one of the scan lines so that the first connecting lines are electrically connected to the first ends of said at least one of the scan lines through the contact hole.

[CLAIMS 7]

The display device of claim 1, wherein the substrate further includes a second connecting part, the second connecting part is formed in a third peripheral area, is coupled with second ends of the scan lines and includes a plurality of third groups disposed in second layers different from each other, the third peripheral area is adjacent to the second ends of the scan lines, the scan driving signal is applied to the second connecting part.

[CLAIMS 8]

The display device of claim 7, wherein the first connecting part is electrically coupled with odd numbered scan lines, and the second connecting part is electrically coupled with even numbered scan lines.

[CLAIMS 9]

A method of manufacturing a liquid crystal display device, the method comprising:

forming a plurality of scan lines, a plurality of scan electrode extended from the scan lines in display area of a first substrate, and forming a plurality of first scan connecting lines electronically connected with a portion of the scan lines in a peripheral area of the display area;

forming an insulation layer on the first substrate having the scan line, the scan electrode and the first connection lines;

forming a plurality of data lines, a plurality of source and drain electrodes extended from the data lines, and forming a plurality of second connecting lines electronically

connected with the remaining portion of the scan lines in a peripheral area of the display area;

combining the first substrate with a second substrate; and

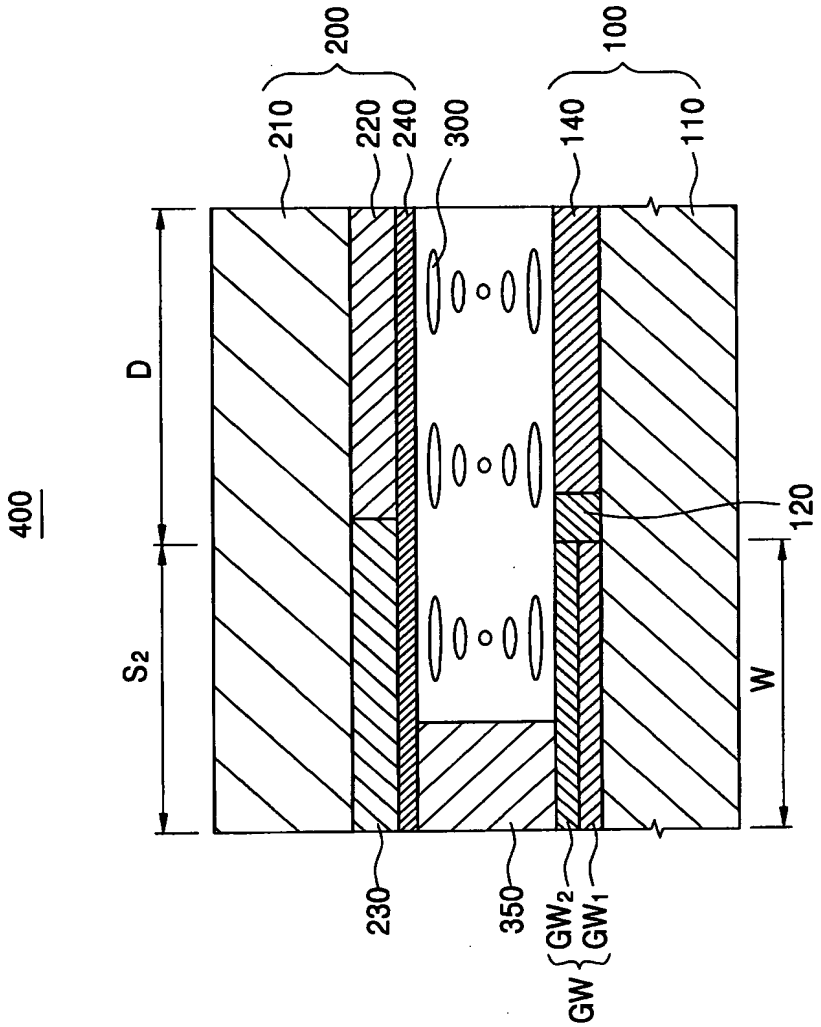
interposing a liquid crystal between the first and second substrates.

[CLAIMS 10]

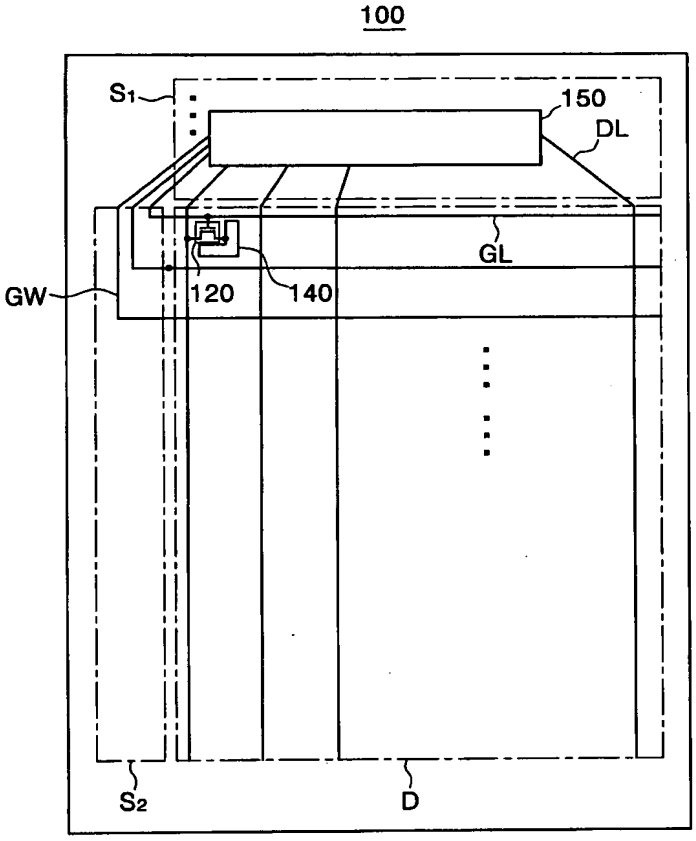
The method of manufacturing in claim 9, further comprising forming a contact hole for exposing the remaining portion of the scan lines in the insulation layer before forming the second connecting lines.

**[DRAWING]**

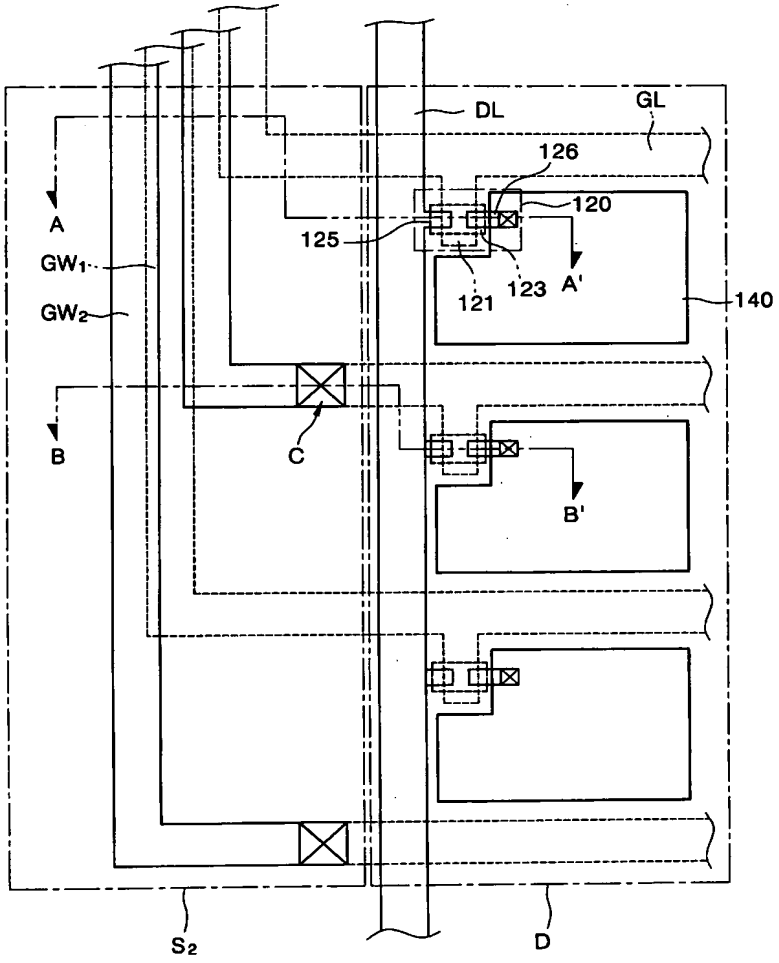
[FIG.1]



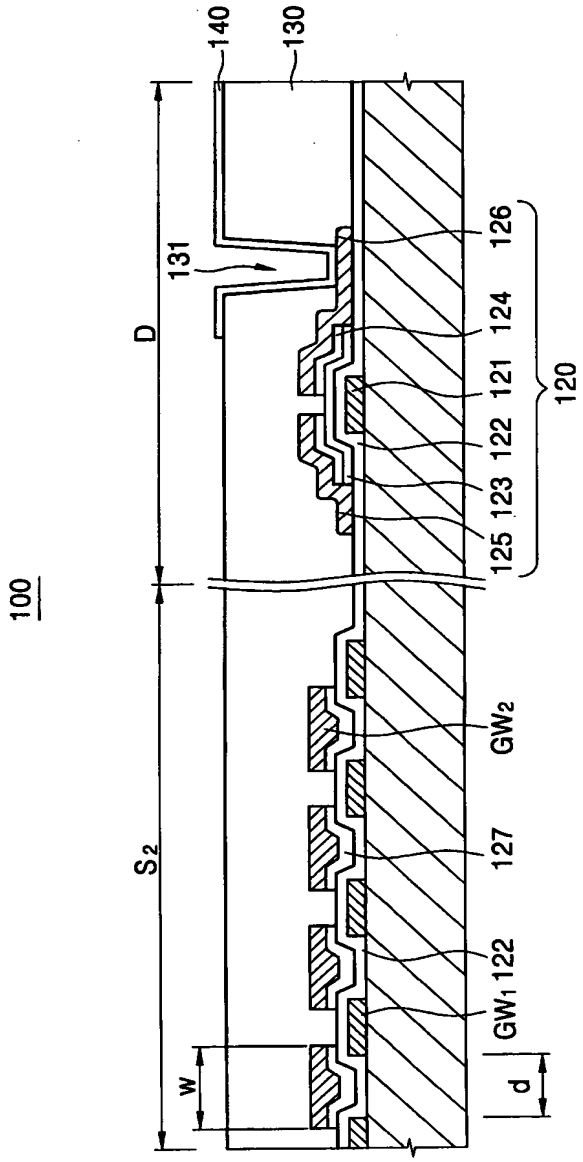
[FIG.2]



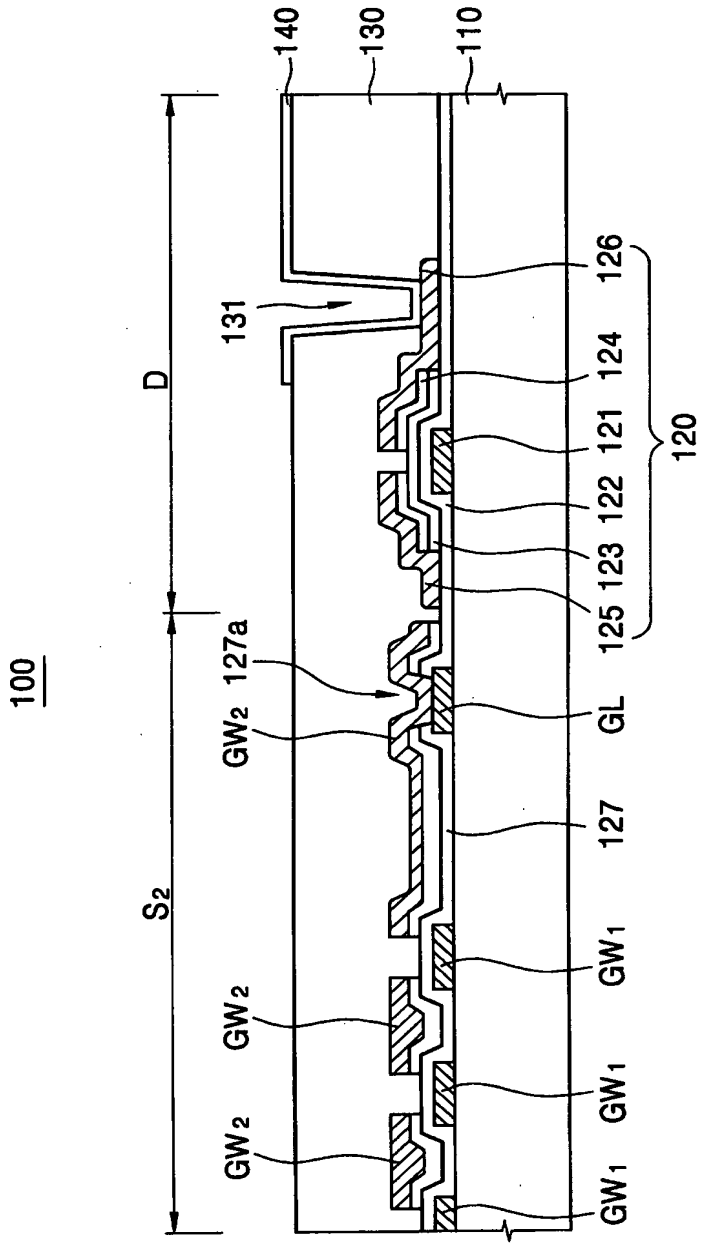
[FIG.3]



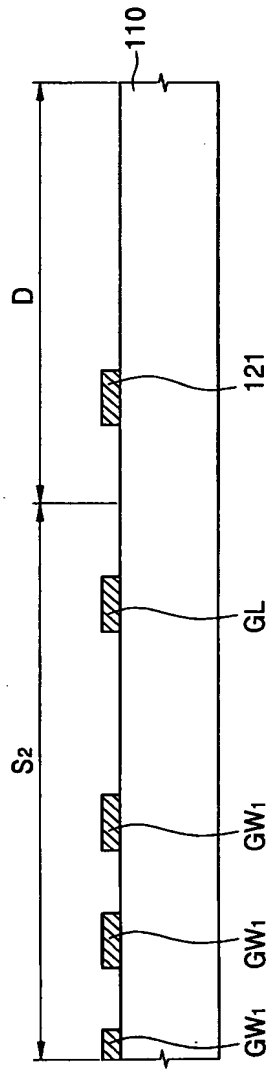
[FIG.4]


100
140
130
131
D
126
124
121
122
123
125
120
$GW_2$
127
$S_2$
122
$GW_1$
w
d

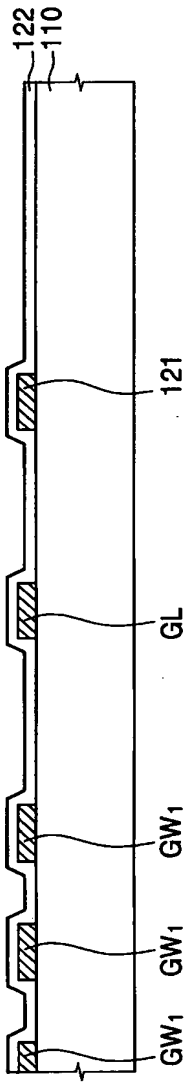
[FIG.5]


100
140
130
110
D
131
126
124
121
122
123
125
120
127a
GW2
GL
127
S2
GW1
GW2
GW1
GW2
GW1

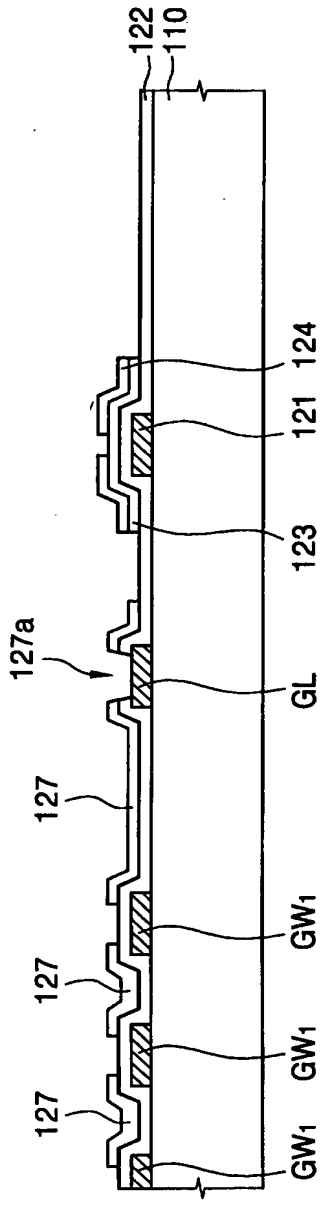
[FIG.6A]



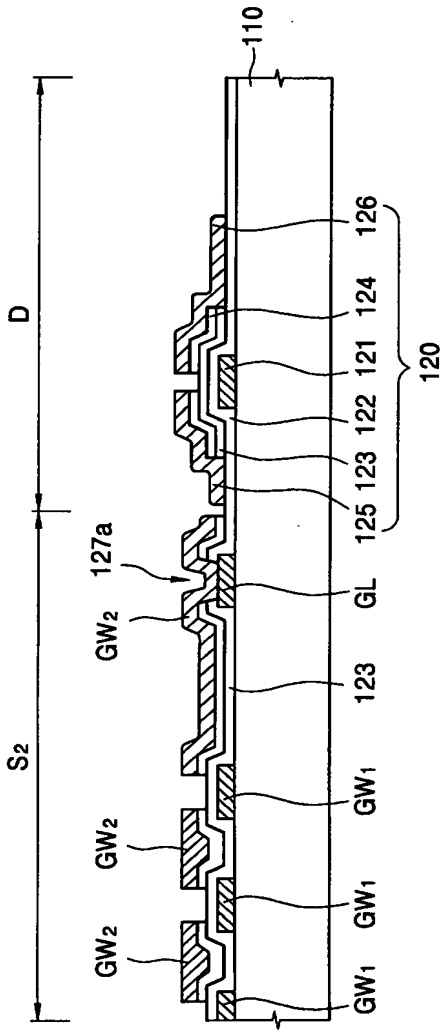
[FIG.6B]



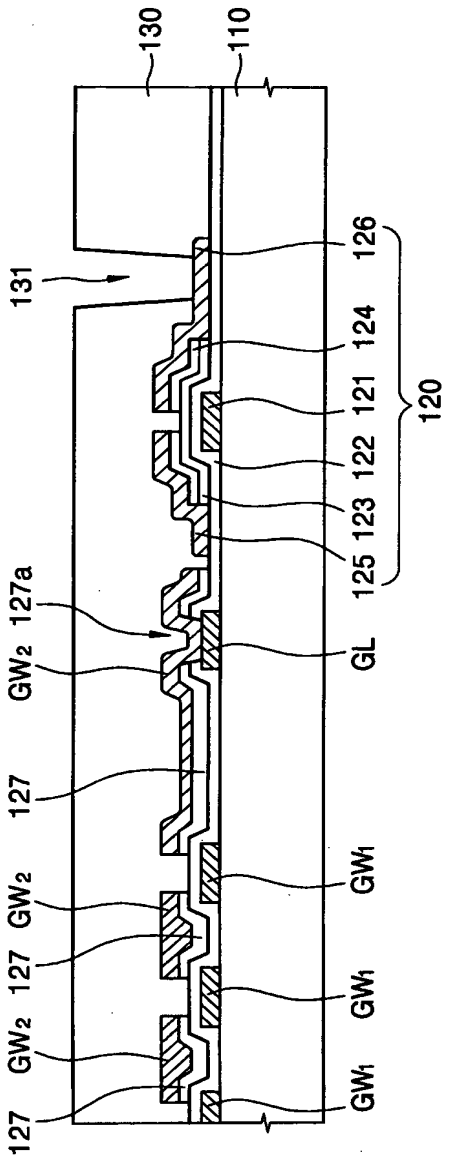
[FIG.6C]



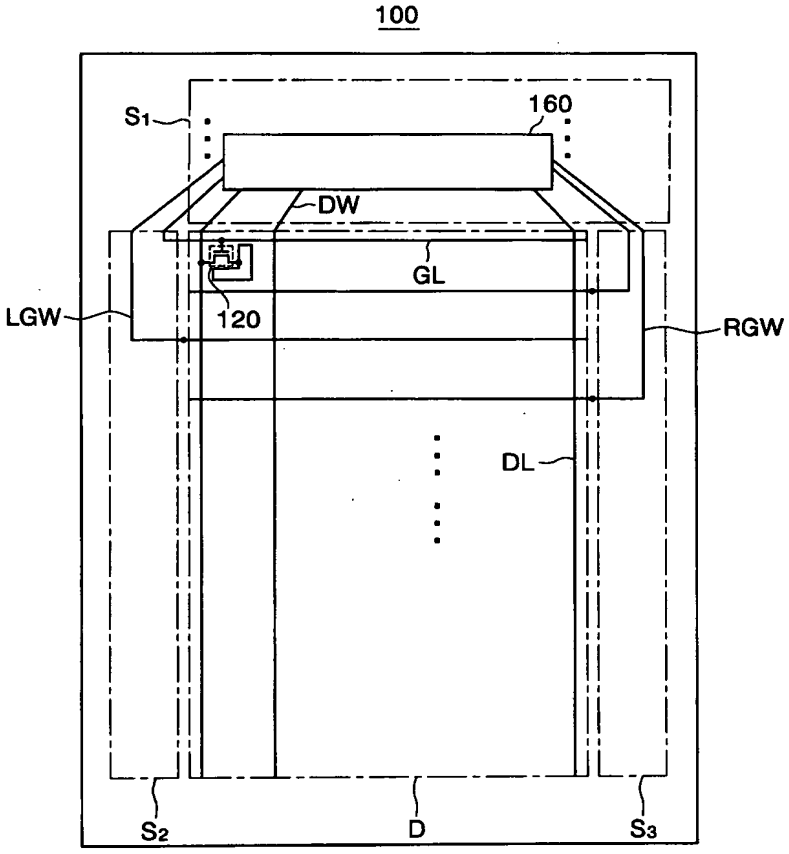
[FIG.6D]


110
D
126
124
121
122
123
125
120
127a
GW2
GL
123
S2
GW1
GW2
GW1
GW2
GW1

[FIG.6E]


130
110
131
126
124
121
122
123
125
120
127a
GW2
GL
127
GW2
GW1
127
GW2
GW1
127
GW1

[FIG.7]



[FIG.8]